## AMENDMENTS TO THE CLAIMS

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

Listing of Claims:

1. (Previously Presented) A semiconductor device having a metal silicide contact structure, comprising:

a silicon-containing substrate having an insulation layer thereon, the insulation layer having an opening that exposes a portion of the silicon-containing substrate;

a metal silicide layer in the opening of the insulation layer and directly on the silicon-containing substrate; and

a silicon-containing conductive layer directly on the metal silicide layer,

wherein the metal silicide layer has a thickness of less than about 100 Å and includes silicon from both the silicon-containing substrate and the silicon-containing conductive layer.

2. (Original) A semiconductor device having a metal silicide contact structure as claimed in claim 1, wherein the conductive layer is a semiconductor layer.

3. (Original) A semiconductor device having a metal silicide contact structure as claimed in claim 1, wherein the metal silicide layer is formed using a native metal silicide having a first phase and a second phase, the second phase having a first stoichiometrical composition ratio that is different from a second stoichiometrical composition ratio of the first phase.

4. (Original) A semiconductor device having a metal silicide contact structure as claimed in claim 1, wherein the substrate is comprised of a material selected from the group consisting of silicon, silicon germanium, silicon-on-insulator (SOI), and silicon-germanium-on-insulator (SGOI).

5. (Original) A semiconductor device having a metal silicide contact structure as claimed in claim 1, further comprising a silicon layer or a silicon germanium layer in a form of a crystalline phase or an amorphous phase formed on the substrate.

6. (Original) A semiconductor device having a metal silicide contact structure as claimed in claim 1, wherein the conductive layer comprises a silicon layer or a silicon germanium layer in a form of a crystalline phase or an amorphous phase.

7. (Original) A semiconductor device having a metal silicide contact structure as claimed in claim 1, wherein the conductive layer is doped polycrystalline silicon.

8. (Original) A semiconductor device having a metal silicide contact structure as claimed in claim 1, wherein the metal silicide layer has a resistance between about 3 to 20 Ω/□.

9. (Original) A semiconductor device having a metal silicide contact structure as claimed in claim 1, further comprising a gate oxide film formed on the substrate.

10. (Original) A semiconductor device having a metal silicide contact structure as claimed in claim 9, further comprising a gate stack formed on the gate oxide film.

11. (Original) A semiconductor device having a metal silicide contact structure as claimed in claim 10, further comprising gate sidewall spacers formed on the sides of the gate stack.

12. (Original) A semiconductor device having a metal silicide contact structure as claimed in claim 9, further comprising a source/drain area formed on the substrate exposed by the opening in the insulation layer.

13. (Original) A semiconductor device having a metal silicide contact structure as claimed in claim 1, further comprising:

field oxide films formed on the substrate; and

a pad layer formed between the field oxide films and below the metal silicide layer.

14. (Original) A semiconductor device having a metal silicide contact structure as claimed in claim 13, and further comprising:

a second insulation layer formed above the field oxide films and the pad layer;

a bit line stack formed on the second insulation layer; and

a third insulation layer formed on the bit line stack and the second insulation layer.

15. (Cancelled).

16. (Original) A semiconductor device having a metal silicide contact structure as claimed in claim 1, wherein the conductive layer is a metallic material.

17. (Previously Presented) A semiconductor device having a metal silicide contact structure as claimed in claim 1, further comprising a metal layer formed on the conductive layer.

18. (Previously Presented) A semiconductor device having a metal silicide contact structure, comprising:

a silicon-containing substrate;

a gate oxide film on the silicon-containing substrate;

a gate stack on the gate oxide film, the gate stack including a silicon-containing material at an upper surface of the gate stack;

a metal silicide layer directly on the silicon-containing substrate in a contact area adjacent to the gate stack, and directly on the silicon-containing material of the gate stack; and

a silicon-containing capping layer directly on the metal silicide layer, wherein:

the metal silicide layer has a thickness less than about 100 Å,

the metal silicide layer directly on the silicon-containing substrate includes silicon from both the silicon-containing substrate and the silicon-containing capping layer, and

the metal silicide layer directly on the silicon-containing material of the gate stack includes silicon from both the silicon-containing material of the gate stack and the silicon-containing capping layer.

19. (Original) A semiconductor device having a metal silicide contact structure as claimed in claim 18, further comprising:

a source/drain area formed on the substrate;

a lightly-doped source/drain area formed on the substrate between the metal silicide layer formed on the substrate and the gate oxide film; and

gate sidewall spacers formed on sides of the gate stack.

Claims 20-43. (Cancelled).

44. (New) A semiconductor device having a metal silicide contact structure as claimed in claim 1, wherein a lower portion of the metal silicide layer is within the silicon-containing substrate and an upper portion of the metal silicide layer is within the silicon-containing conductive layer.

45. (New) A semiconductor device having a metal silicide contact structure as claimed in claim 1, wherein:

the metal silicide layer has an uppermost extent and a lowermost extent,

the uppermost extent of the metal silicide layer is above a first surface of the silicon-containing substrate, and

the lowermost extent of the metal silicide layer is below the first surface of the silicon containing substrate.

46. (New) A semiconductor device having a metal silicide contact structure as claimed in claim 45, wherein the first surface of the silicon-containing substrate corresponds to a substantially planar major surface of the silicon-containing substrate.

47. (New) A semiconductor device having a metal silicide contact structure as claimed in claim 18, wherein a lower portion of the metal silicide layer in the contact area is within the silicon-containing substrate and an upper portion of the metal silicide layer in the contact area is within the silicon-containing conductive layer.

48. (New) A semiconductor device having a metal silicide contact structure as claimed in claim 18, wherein the silicon-containing capping layer is directly on the metal silicide layer in the contact area.

49. (New) A semiconductor device having a metal silicide contact structure as claimed in claim 48, wherein:

the metal silicide layer in the contact area has an uppermost extent and a lowermost extent,

the uppermost extent of the metal silicide layer is above a first surface of the silicon-containing substrate, and

the lowermost extent of the metal silicide layer is below the first surface of the silicon containing substrate.

50. (New) A semiconductor device having a metal silicide contact structure as claimed in claim 49, wherein the first surface of the silicon-containing substrate corresponds to a substantially planar major surface of the silicon-containing substrate.